In this response, Applicant traverses the §102(b) and §103(a) rejections.

With regard to independent claims 1 and 36, each of these claims calls for a comparator circuit having an evaluation element and first and second input legs coupled thereto, with the first and second input legs being adapted to receive respective first and second input signals, and with the evaluation element being adapted to perform a comparison of the first and second input signals. Claims 1 and 36 further specify that each of the first and second legs has "associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals." Claim 1 further specifies that the first and second input legs have "non-complementary structures relative to one another." Claim 36 further specifies that the first and second input signals are "non-complementary input signals."

An example of the claimed arrangement is shown in FIG. 11 of the drawings, and described as follows in the specification at page 15, line 14 to page 16, line 8, with emphasis supplied:

> FIG. 11 shows a basic non-complementary comparator circuit in accordance with an illustrative embodiment of the invention. . . . The circuit includes a cross-coupled RAM cell formed of transistors m1, m2, m3 and m4.
>
> Inputs in_1 and in_2 are applied to evaluation legs denoted as R_1 and R_2 respectively. As previously noted, evaluation legs are also referred to herein as input legs. In accordance with the invention, these legs have input structures which are non-complementary relative to one another, and therefore do not behave as conventional digital circuit structures. The input legs are coupled to nodes of the RAM cell, e.g., nodes *out* and *outn* in this illustrative circuit. . . .
>
> The evaluation legs in the basic comparator circuit of FIG. 11 are viewed as variable resistances during evaluation. More particularly, the variable resistance associated with left leg R_1 is a function of input in_1 and the variable resistance associated with right leg R_2 is a function of input in_2, as is shown in the figure. The outputs *out* and *outn* of the FIG. 11 comparator circuit are a function of the variable resistances as follows:

If ($R_1 < R_2$), the circuit will evaluate to *out* = 1 and *outn* = 0.

If ($R_1 > R_2$), the circuit will evaluate to *out* = 0 and *outn* = 1.

In this embodiment, the evaluation occurs when the clock signal ck goes low, although this is of course by way of example and not a requirement of the invention.

The FIG. 11 comparator circuit by virtue of the variable resistances R_1 and R_2 is able to compare input signal in_1 against input signal in_2, even though in_1 may not be the complement of in_2. In other words, if the binary weight of in_1 is greater than the binary weight of in_2, $R_1 < R_2$ and *out* = 1, thereby indicating that $in_1 > in_2$. As noted previously, conventional comparators are generally unable to process non-complementary inputs in this manner. The variable resistances may be implemented using weighted arrays of transistors, as will be described below.

The present invention as set forth in claims 1 and 36 is thus directed to a particularly advantageous comparator circuit arrangement that is capable of comparing non-complementary input signals. As noted above, conventional comparator circuits are unable to compare non-complementary input signals.

Applicant respectfully submits that such an arrangement is not taught or suggested by the Pascucci reference. More particularly, as will be described below, Pascucci fails to teach or suggest an arrangement in which an evaluation element is adapted to perform a comparison of first and second input signals applied to respective first and second input legs as claimed. Pascucci therefore fails to provide the significant advantages associated with the claimed arrangement in terms of its ability to compare non-complementary input signals.

Applicant notes that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson

v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicant submits that the Examiner has failed to establish anticipation of at least independent claims 1 and 36 by the Pascucci reference.

The Examiner in formulating the §102(b) rejection argues that the claimed evaluation element corresponds to virtual ground latch structure 2 of Pascucci FIG. 2, and that the claimed first and second input legs correspond to the respective left branch 8 and right branch 9 coupled to respective nodes B and B′ in Pascucci FIG. 2 (Final Office Action, page 3, section 4). The Examiner further argues that the claimed first and second input signals correspond to the current signals Il and Ir referred to in column 4, lines 52-56 of Pascucci (Final Office Action, page 4, section 7).

However, as indicated previously, claims 1 and 36 call for first and second input legs adapted to receive respective first and second input signals, but the Il and Ir current signals are not input signals in the Pascucci device. These signals are not supplied as inputs to the Pascucci device. Instead, Il and Ir are simply used to identify currents flowing through the respective branches 8 and 9.

Also as indicated previously, claims 1 and 36 further specify that each of the first and second legs has "associated therewith a variable parameter having a value that is a function of a corresponding one of the input signals." This limitation is clearly not met if one attempts to characterize the Il and Ir current signals as the claimed input signals, since there is no variable parameter in either branch 8 or 9 that is a function of the respective current signal Il or Ir. Instead, Pascucci indicates that the currents Il and Ir are themselves functions of applied input signals associated with buses denoted YM and YN.

Moreover, Pascucci specifically teaches away from the claimed arrangement by indicating that the buses YM and YN collectively characterize a "selection means" which "provides the ability to select a memory cell from the memory cell matrix" comprising memory cells 16 and 17 (Pascucci, column 3, lines 34-43). The FIG. 2 circuit thus does not compare input signals, but instead determines if particular ones of the memory cells 16 and 17 are programmed or unprogrammed (Pascucci, column 5, line 39 to column 6, line 3).

Applicant submits that the virtual ground latch structure 2, which the Examiner has characterized as corresponding to the claimed evaluation element, is not adapted to perform a

comparison of any input signals associated with the buses YM and YN. In other words, the input signals YM and YN shown in Pascucci FIG. 2 are not compared by the virtual ground latch structure 2. Moreover, there are no other input signals in Pascucci that are applied to left branch 8 and right branch 9 and which are compared by the virtual ground latch structure 2. As noted above, the current signals Il and Ir cannot reasonably be characterized as the claimed input signals, without violating other requirements of the claim language.

Pascucci therefore fails to teach or suggest at least the limitation of claims 1 and 36 regarding an evaluation element of a comparator circuit being adapted to perform a comparison of first and second input signals applied to respective first and second input legs. Pascucci thus fails to teach or suggest "each and every element" of claims 1 and 36 in "as complete detail" as is contained in those claims. The §102(b) rejection is therefore believed to be improper, and should be withdrawn.

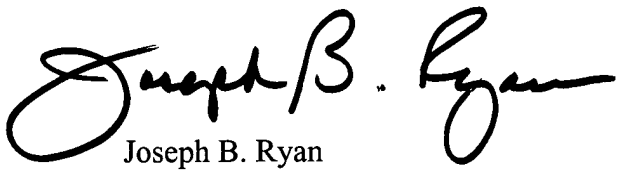
Dependent claims 2-7 are believed allowable for at least the reasons identified above with regard to their corresponding independent claim 1. Moreover, one or more of these claims are believed to define separately-patentable subject matter relative to Pascucci and the other art of record. For example, dependent claim 3 specifies that the "variable parameter having a value that is a function of a corresponding one of the input signals" comprises a variable resistance. An example is the variable resistance $R_1 = F(in_1)$ or $R_2 = F(in_2)$ as described previously herein in conjunction with FIG. 11 of the drawings. There is no such variable resistance, having a value which is a function of an input signal, associated with either of the branches 8 or 9 in Pascucci.

Independent claim 37 includes limitations similar to those of claim 1, and is therefore believed allowable for at least the reasons identified above with regard to claim 1. The §103(a) rejection is thus also believed to be improper, and should be withdrawn.

In view of the above, Applicant believes that claims 1-7, 36 and 37 are in condition for allowance, and respectfully requests withdrawal of the §102(b) and §103(a) rejections.

As mentioned previously, a Notice of Appeal is submitted concurrently herewith.

Respectfully submitted,



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Enclosure(s): Notice of Appeal